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H01L 21/336 21/30 29/786

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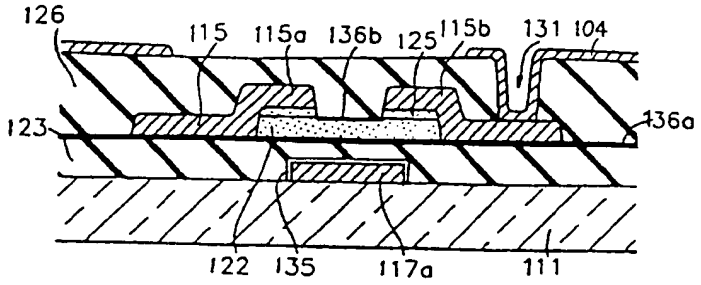
(58) Field of Search
UK CL (Edition O) H1K KCAA KJACX KJAX
INT CL[6] H01L
Online:WPI,JAPIO,CLAIMS,INSPEC

(54) Thin film transistor

(57) The use of an organic layer in a TFT results in problems in the performance of a LCD. A plasma treatment, using O, N or a gas containing N or F, of the semiconductor layer (122) and the organic gate insulation layer (123) prevents detachment between the layers and the creation of charge traps at the interface including the semiconductor layer 50 that the aperture ratio of the LCD can be improved without deteriorating the TFT ON characteristic.

FIG. 16H



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This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

FIG. 1
PRIOR ART

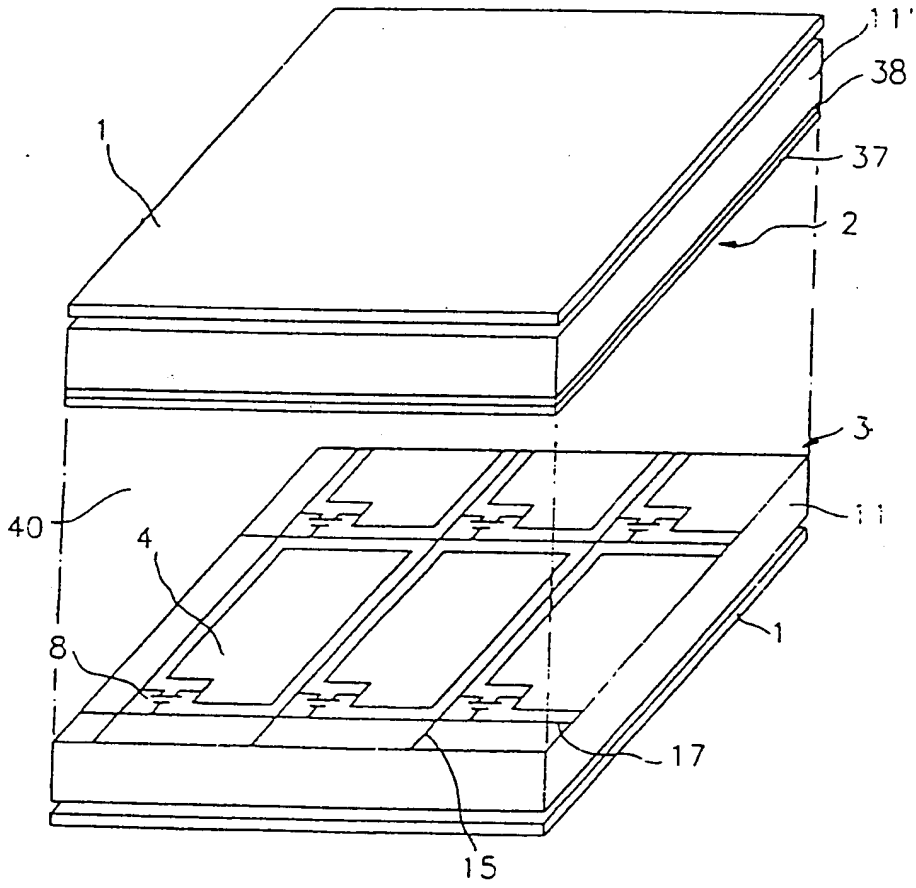


FIG. 2
PRIOR ART

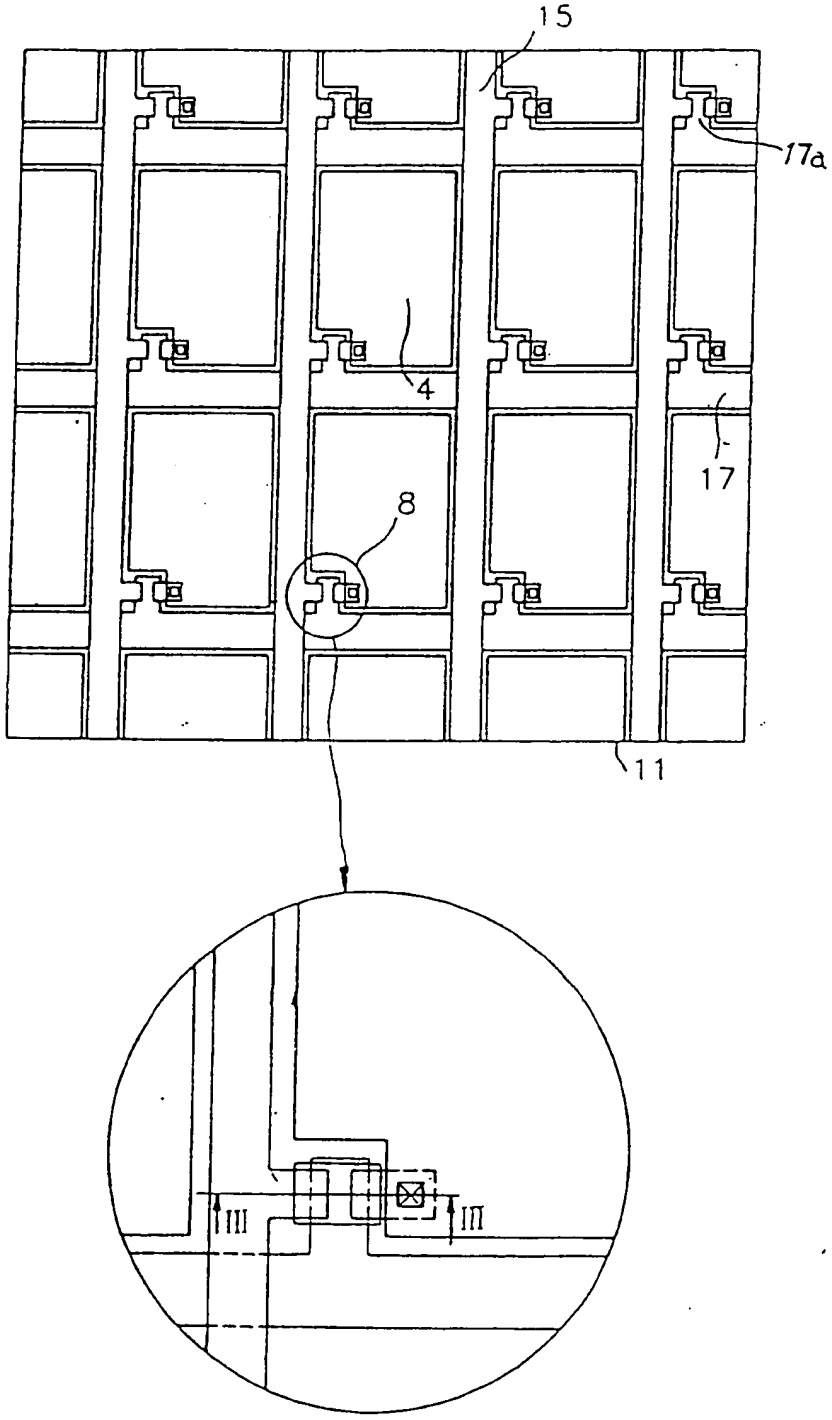


FIG. 3
PRIOR ART

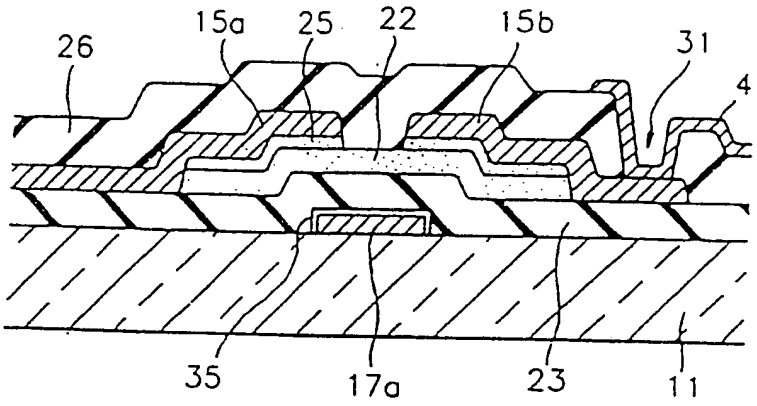


FIG. 4
PRIOR ART

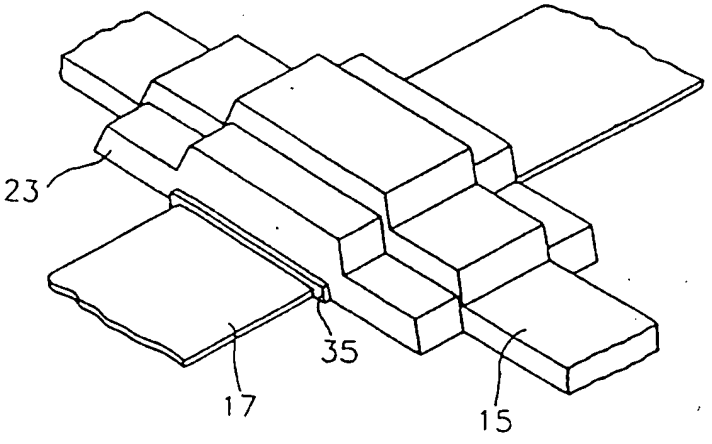


FIG. 5
PRIOR ART

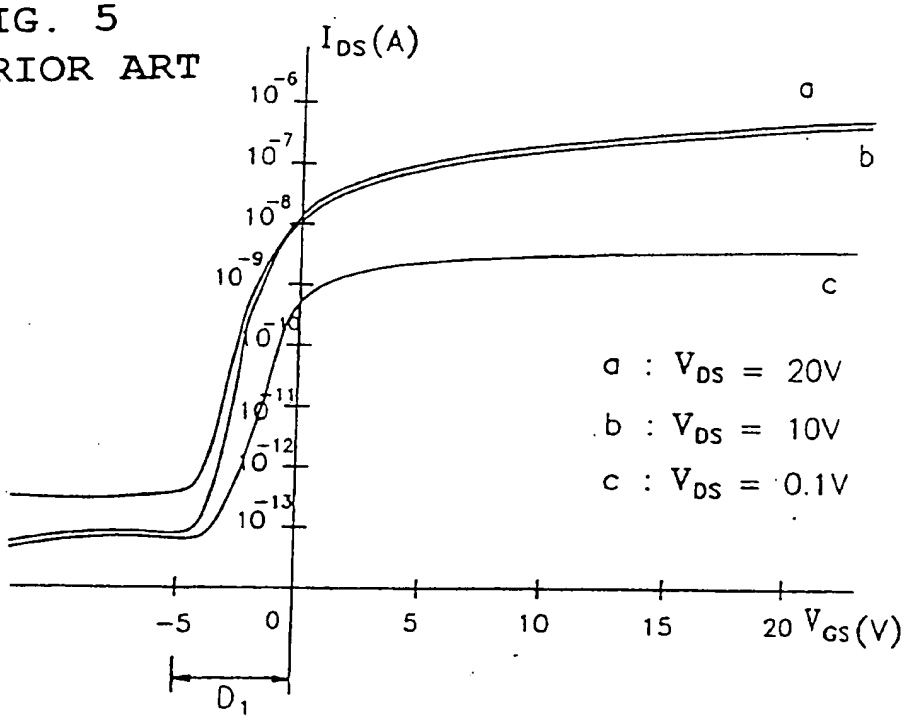


FIG. 9

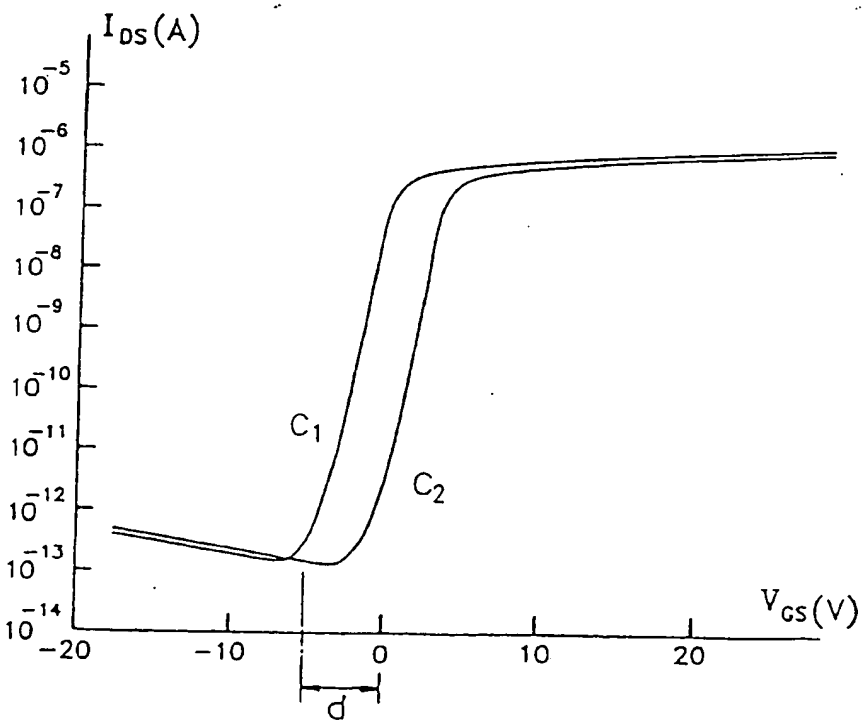


FIG. 6

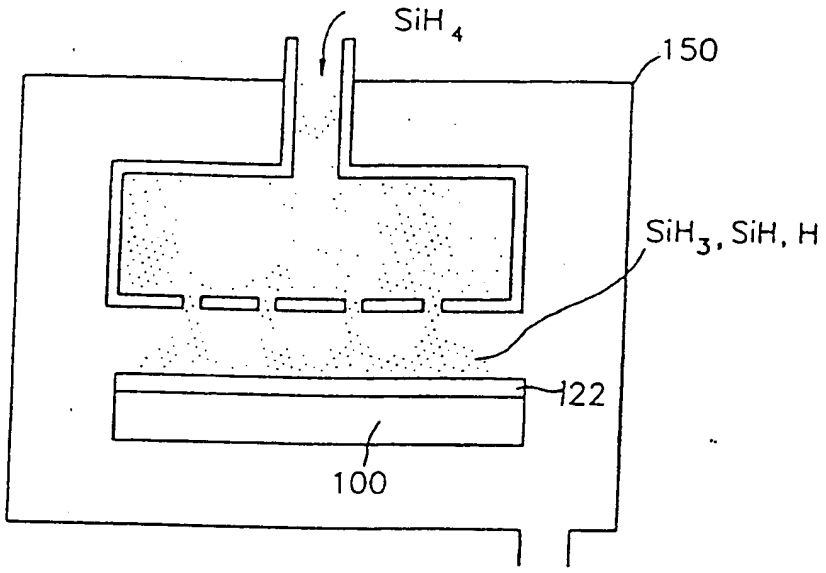


FIG. 7

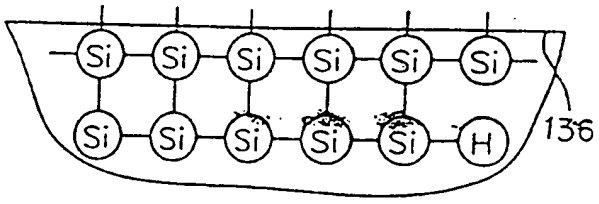
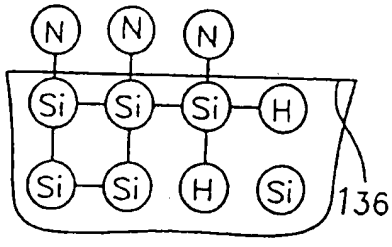


FIG. 8



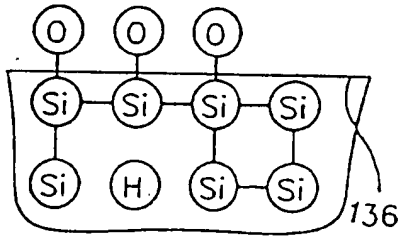


FIG. 10

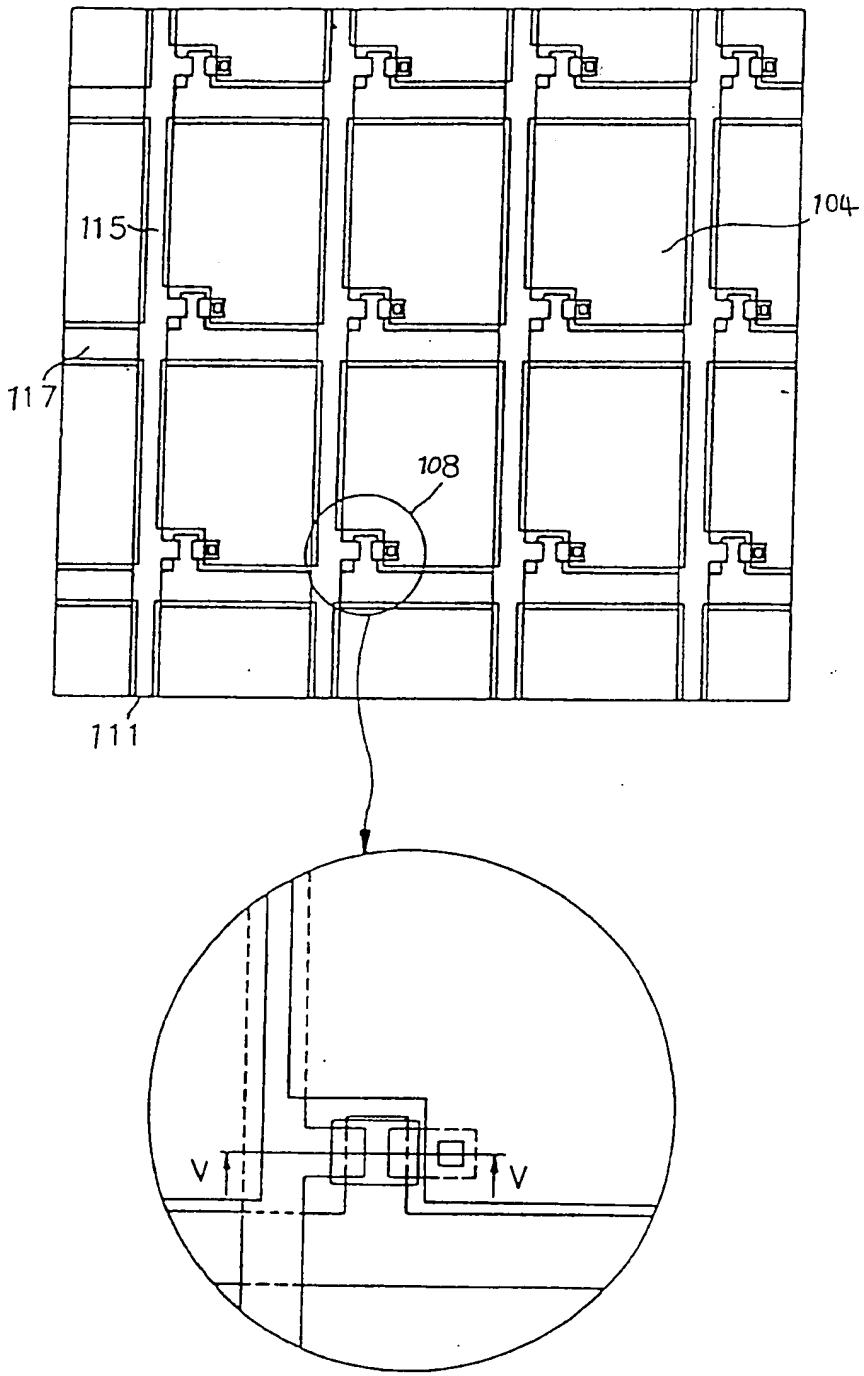


FIG. 11A

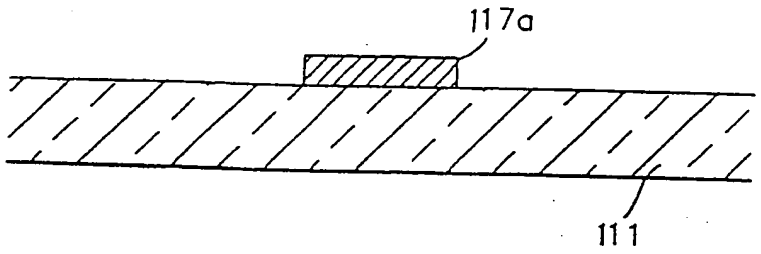


FIG. 11B

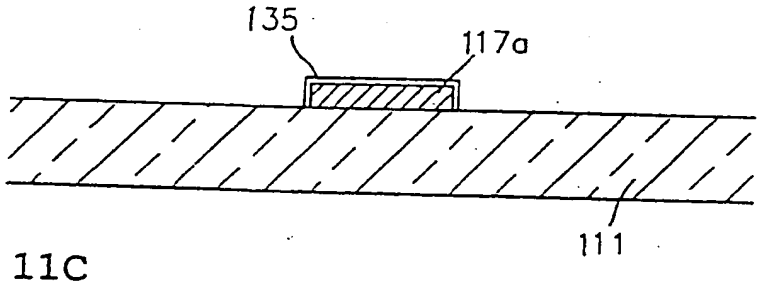


FIG. 11C

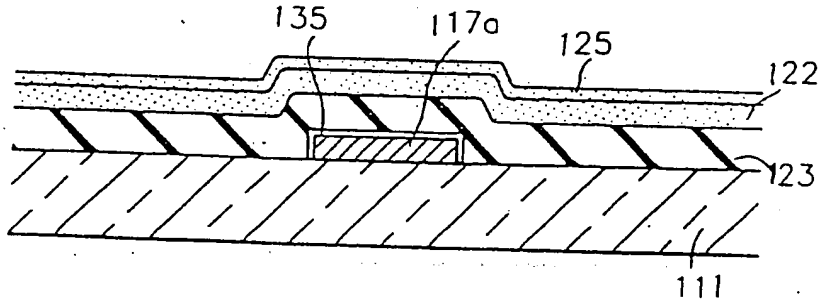


FIG. 11D

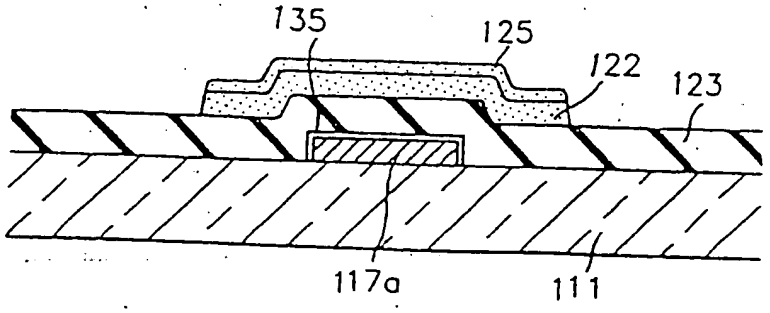


FIG. 11E

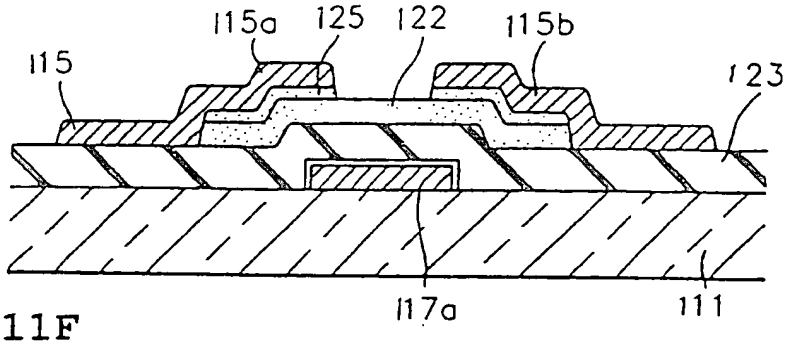


FIG. 11F

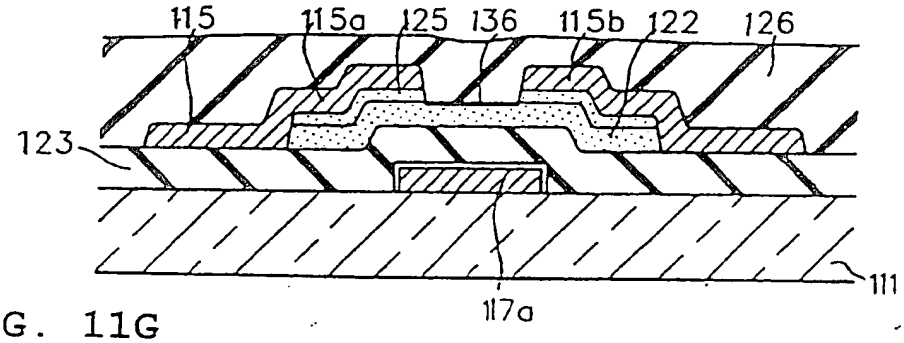


FIG. 11G

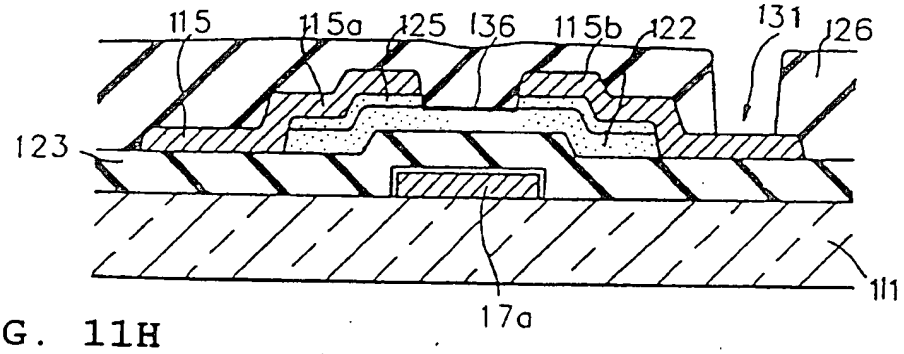


FIG. 11H

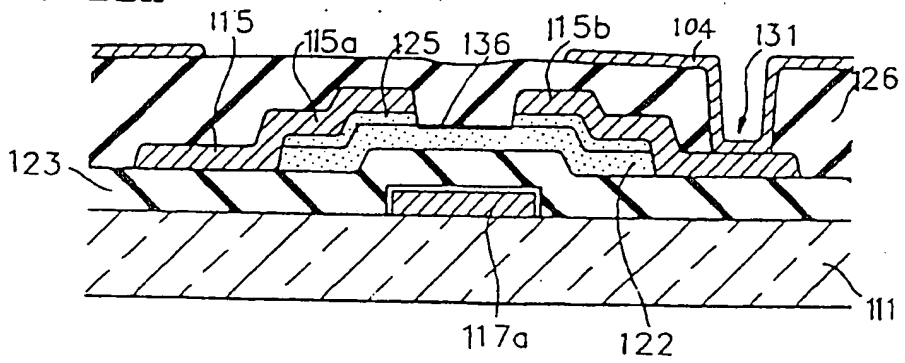


FIG. 12A

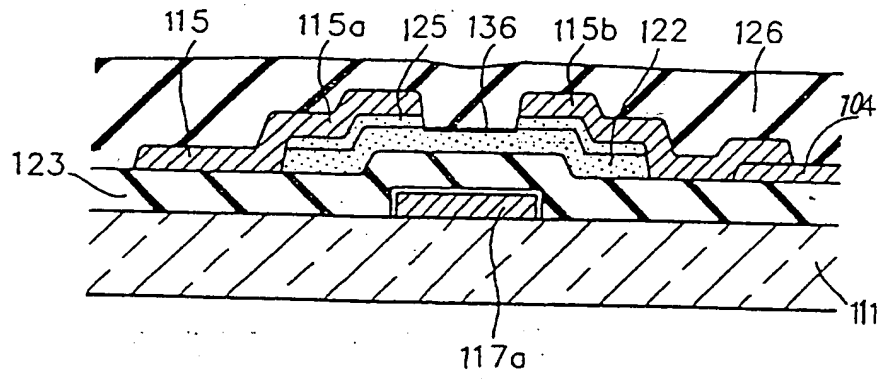


FIG. 12B

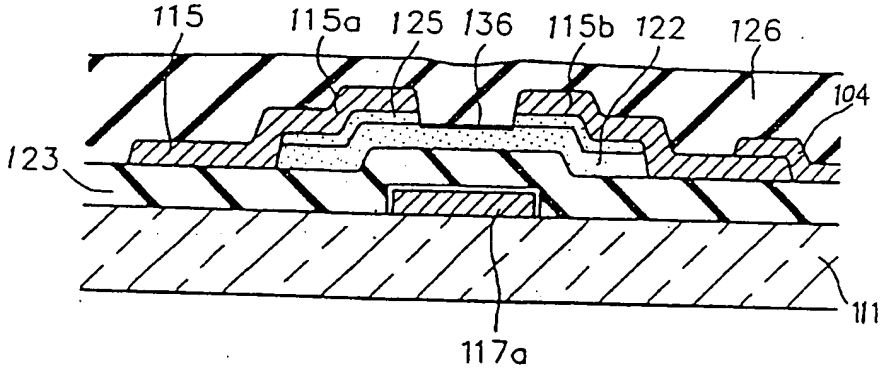


FIG. 13

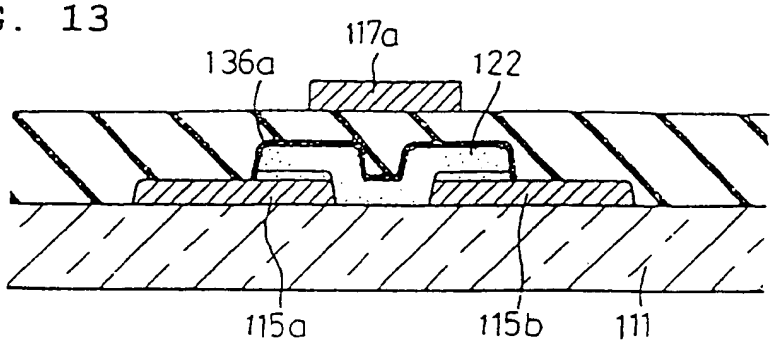


FIG. 14

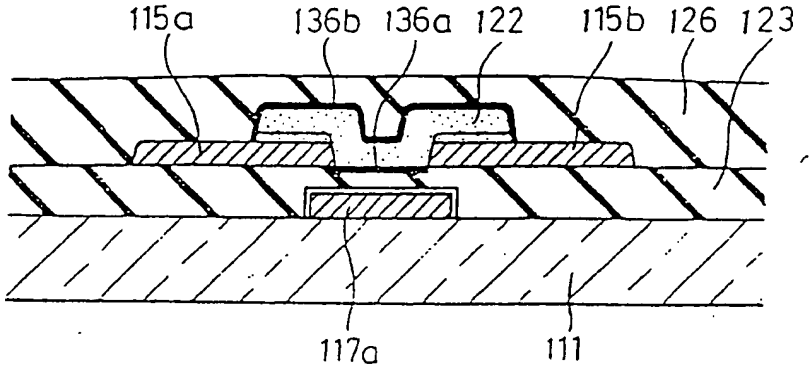


FIG. 15

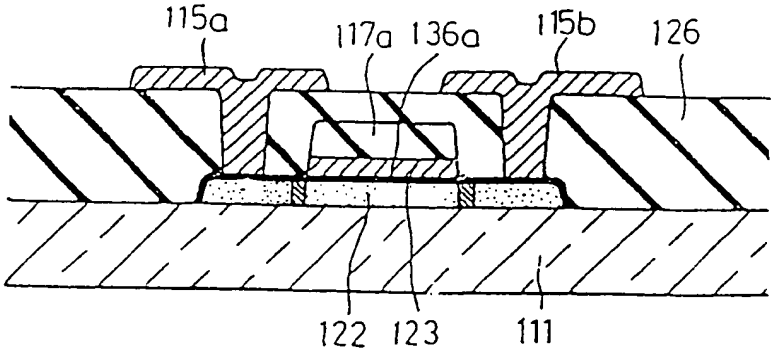


FIG. 16A

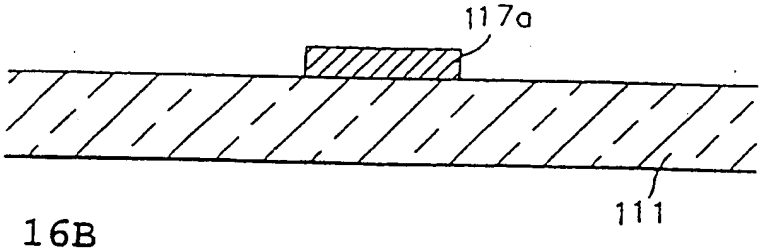


FIG. 16B

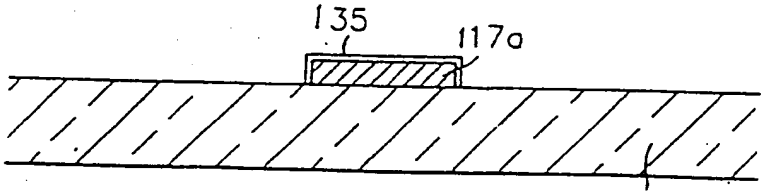


FIG. 16C

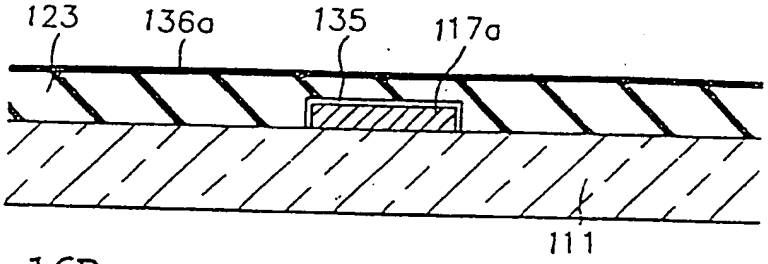


FIG. 16D

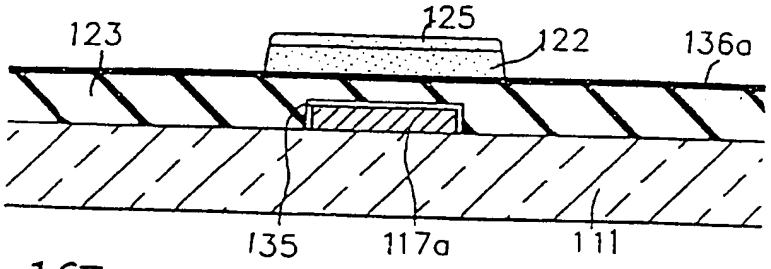


FIG. 16E

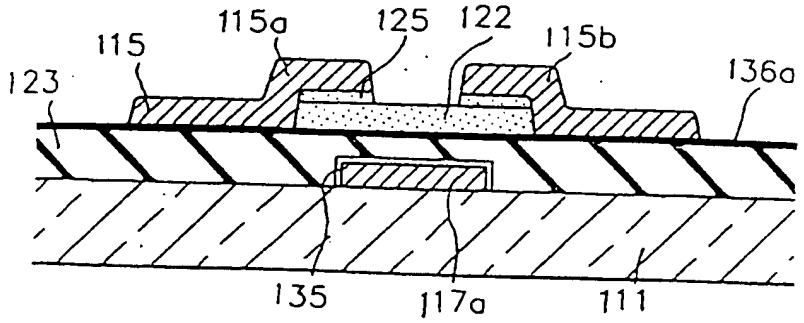


FIG. 16F

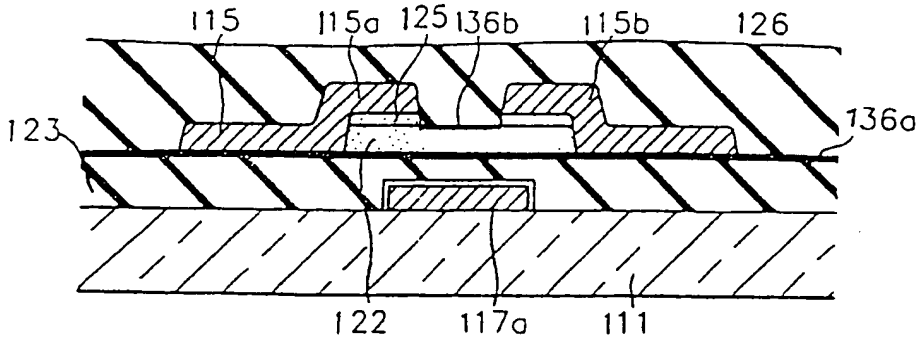


FIG. 16G

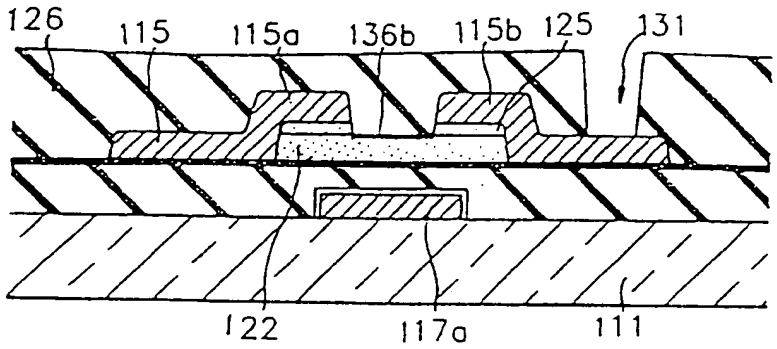


FIG. 16H

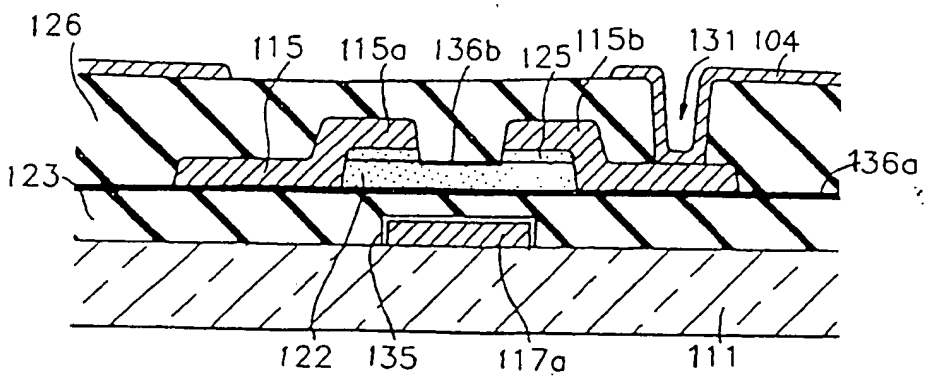


FIG.17A

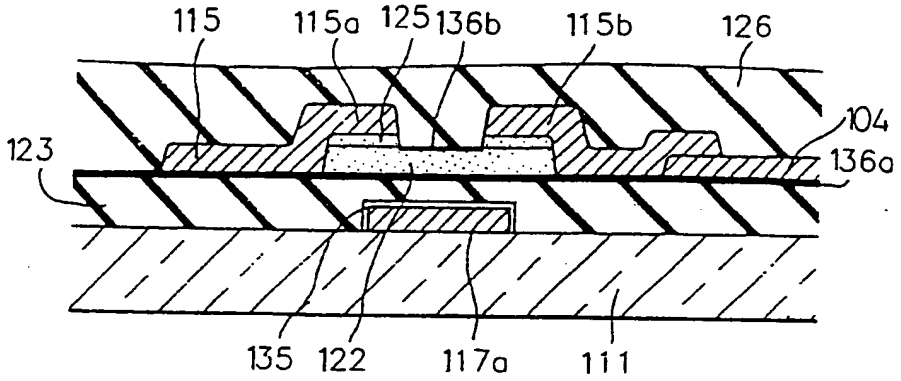
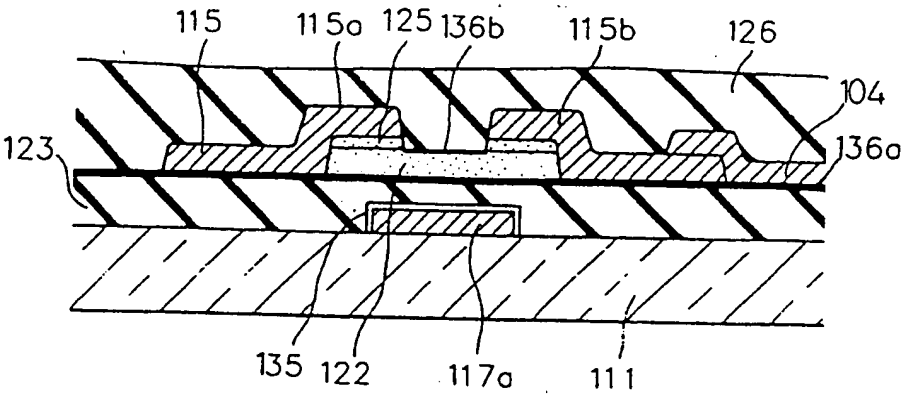


FIG.17B



A method of manufacturing an active matrix liquid crystal display and the structure of the liquid crystal display manufactured by the same method.

The present invention relates to an active matrix liquid crystal display (AMLCD) having a thin film transistor (TFT) as a switching element, and more particularly to the method of manufacturing the TFT and the structure of the TFT manufactured by the same method.

In a conventional active matrix liquid crystal display as shown in FIG.1, the structure of a conventional AMLCD includes two substrates (a first and a second substrate) forming pixels in a matrix array.

On the first substrate 3, each pixel electrode 4 is disposed at the intersection between gate bus lines 17 and data bus lines 15. Gate bus lines 17 are formed in horizontal direction and include gate electrodes (not shown) branched off therefrom. On the other hand, data bus lines 15 are formed in vertical direction and include data electrodes (not shown) branched off therefrom. At the intersections between gate bus lines and data bus lines, TFTs 8 are disposed and make electrical contact with pixel electrodes 4.

On the second substrate 2, color filter layers 38 and a common electrode 37 are formed.

The first and the second substrates are correspondingly

arranged in a position to face each other and are bonded together. The space between the substrates is filled with a liquid crystal material 40 to complete an active matrix liquid crystal panel. The polarizing plate 1 is formed on the outer side of the substrates before the bonding, and 11 and 11' in Fig.1 represent transparent glass substrates.

The structure and the method of manufacture of the first substrate 3, which is directed to the present invention, is described in detail with reference to Figs. 2 and 3.

Fig. 2 is a plan view showing the structure of a conventional AMLCD and Fig. 3 is a cross-sectional view taken along the line III-III in Fig. 2.

According to the conventional method of manufacturing an AMLCD, the structure of the AMLCD is as follows. On a transparent glass substrate 11, a gate bus line 17 in horizontal direction and a gate electrode 17a branched off therefrom are formed. The gate electrode may be anodized to improve insulating performance and to prevent hill-lock on the surface. On the substrate 11 including the gate electrode 17a, a gate insulating layer 23 using an inorganic material, such as SiN_x or SiO_2 is formed. On the portion of the gate insulating layer 23 over the gate electrode 17a, a semiconductor layer 22 using amorphous silicon (a-Si) is formed. On the semiconductor layer of a-Si, separated ohmic contact layers 25 using n+ a-Si are formed. On the surface

including the ohmic contact layer 25, a data bus line 15 in vertical direction, a source electrode 15a connected to the data bus line 15 and a drain electrode 15b spaced apart from the source electrode 15a are formed. At the same time, the source 15a and the drain electrode 15b make electrical contact with the corresponding ohmic contact layer 25, respectively.

Then, a protection layer 26 using an inorganic material such as SiN_x covers the substrate including the source 15a and the drain electrode 15b. A pixel electrode 4 using a transparent conductive material such as indium tin oxide (ITO) is formed on the protection layer which makes an electrical contact with the drain electrode 15b through a contact hole 31 formed in the protection layer 26.

However, since the first substrate of the AMLCD results in a TFT and bus lines with stepped surface as shown in FIG. 4, the pixel electrode 4 is formed at a distance away from the gate bus line 17, data bus line 17 and the TFT. This is because an inorganic material such as SiN_x or SiO_2 is used for the gate insulating layer 23 or the protection layer 26

Moreover, the stepped TFT and lines causes problems in the manufacture of an AMLCD. In particular, when an alignment film is formed on the stepped surface, the initial orientation of the liquid crystal becomes inhomogeneous and reduces the quality of the LCD because of the rubbing defect at the stepped portion of the alignment film.

In order to overcome such problems, an organic material with high planarization property is used for the gate insulating layer 23 or the protection layer 26. Then, the reduction in the performance of the LCD can be prevented due to the elimination of the rubbing defect. An improvement in aperture ratio can also be achieved since the pixel electrode 4 may be formed to overlap the bus lines.

Introduction of the organic material in a TFT structure, however, causes other problems. The ON characteristic of a TFT becomes unstable, shifting the curve toward its negative direction (Fig. 5) due to the charge trap at the surface of the semiconductor layer 22 in contact with the organic layer.

An object of the present invention is to provide an AMLCD with a stable TFT using an organic protection and/or insulation layer .

To prevent such problems, according to one aspect of the present invention, the surface of the semiconductor layer is plasma-treated using N_2, O_2 or a gas containing N or F, forming stable bond structure of Si-O or Si-N on the surface. In this manner, the interfacial problems between the semiconductor layer and the organic protection layer such as charge trap and detachment can be eliminated. Similarly, the surface of a gate insulating layer which makes contact with the semiconductor layer and is made of organic material, can also be plasma-treated to prevent the

interfacial problems.

Another object of the present invention is to manufacture the first substrate of an AMLCD including plasma treatment step of the semiconductor layer 22 using N_2, O_2 or a gas containing N or F prior to the coating of the organic protection layer 26 with dielectric constant less than 3.0.

Still another object of the present invention is manufacturing the first substrate of an AMLCD including plasma treatment step of the organic gate insulating layer 23 of BCB, in addition to the plasma treatment step of the semiconductor layer 22, using N_2, O_2 or a plasma gas containing N or F.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

For a better understanding of the present invention, embodiments will now be described by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a perspective view showing the structure of a conventional active matrix liquid crystal display.

FIG. 2 is a plan view showing the structure of a conventional active matrix liquid crystal display.

FIG. 3 is a cross-sectional view showing the structure of a conventional active matrix liquid crystal display,

taken along the line III-III in Fig.2.

FIG. 4 is a perspective view showing a stepped surface at the cross-section between a gate bus line and a data bus line.

FIG. 5 shows the curves of ON characteristic of a TFT using an organic protection layer.

FIG. 6 is a cross-sectional view of a plasma treatment apparatus.

FIG. 7 is a diagram showing the chemical structure of a semiconductor layer having dangling bonds at the surface.

FIG. 8 is a diagram showing the chemical structure of a semiconductor layer, after plasma treatment at the surface using N_2, O_2 or a gas containing N or F.

FIG. 9 shows the curves of ON characteristic of a TFT using an organic protection layer after plasma treatment according to the present invention.

FIG. 10 is a plan view showing the structure of an active matrix liquid crystal display according to the present invention.

FIGs. 11A-H and 12A-B are cross-sectional views showing the manufacturing steps of a first substrate of an active matrix liquid crystal display according to the present invention, taken along the line V-V in FIG. 10.

FIGs. 13 to 15 are cross-sectional views showing a first substrate of an active matrix liquid crystal display with various TFT structure according to the present

invention, taken along the line V-V in FIG. 10.

FIG. 16A-H and 17A-B are a cross-sectional views showing another first substrate of an active matrix liquid crystal display according the present invention, taken along the line V-V in FIG. 10.

The organic material for the protection layer or the gate insulation layer may include BCB or PFCB. However, the examples are given for manufacturing the first substrate of an AMLCD using BCB having dielectric constant less than 3.0 and Si-O bond structure.

The importance of the plasma treatment of the semiconductor layer prior to coating an organic layer according to the present invention is described by reviewing the formation of the semiconductor layer.

As shown in Fig. 6, when silane gas (SiH_4) is introduced and discharged in a plasma apparatus 150, it forms a plasma including $SiH_3^{\bullet}$, $SiH_2^{2\bullet}$ and $H^{\bullet}$ radicals. The reaction of the plasma gas results in deposition of an amorphous silicon layer (a-Si:H) 122 on the substrate 100. The semiconductor layer of a-Si:H forms the chemical structure as shown in Fig. 7 including a bonding defect of dangling bonds at the surface.

When the semiconductor layer 122 including such a bond defect is coated with an organic protection layer by spin-coating, the unstable surface of the semiconductor layer results in a poor bondability to the organic layer and

detachment of the organic layer. Moreover, the dangling bond at the surface of the semiconductor layer causes charge trap of electron to shift the TFT ON characteristic curves towards negative voltage direction (Fig. 5). This results in an unstable TFT, undesirably driving a circuit at a voltage lower than the TFT ON voltage.

Thus, the surface 136 of the semiconductor layer is plasma treated by N_2, O_2 or a gas containing N or F to prevent bonding defects and detachment of the semiconductor layer from the organic layer thereon. The surface treatment of the semiconductor layer by N_2, O_2 or a gas containing N or F results in a stable bond structure such as Si-N or Si-O as shown in Fig. 8. Therefore, coating an organic layer on the surface 136 of the semiconductor layer 122 having Si-O or Si-N bond allows a stable bonding between the semiconductor layer and the organic layer eliminating detachment at the interface and providing a stable TFT ON characteristic.

The experimental result of the TFT ON characteristic after coating an organic protection layer such as BCB on the semiconductor layer shows that the characteristic curve after plasma treatment (C2) with N_2, O_2 or a gas containing N or F reveals an improved TFT ON characteristic without shifting (d) compared with the characteristic curve without plasma treatment (C1), as shown in Fig. 9.

Example 1

The method of manufacturing the first substrate of an AMLCD is explained with reference to Fig. 10 showing a plan view of the first substrate of an AMLCD according to the present invention, and Fig. 11 showing a cross-sectional view taken along the line V-V in Fig. 10.

A metal layer, using Al, Al-Ta, Al-Mo, Ta or Ti (being able to be anodized) or Cr, is deposited on a transparent glass substrate 111 and patterned to form a gate bus line and gate electrode 117a branched off therefrom (FIG. 11A). When, the metal layer is able to be anodized an anodized layer 135 is formed on the gate bus line and the gate electrode 117a in order to improve the insulating property and to prevent hill-lock (Fig. 11B).

Then, the overall surface is deposited with an inorganic material such as SiN_x or SiO_2 to form a gate insulation film and a-Si and n$^+$ a-Si are sequentially deposited on the insulating layer 123 (Fig.11C). The a-Si and n$^+$ a-Si are patterned together to form a semiconductor layer 122 and ohmic contact layer 125 (FIG. 11D). Then, a metal such as Al alloy is deposited on the ohmic contact layer 125 and patterned to form a data bus lines 115, a source electrode 115a branched off from the data line, and drain electrode 115b as an output terminal. The exposed portion of the ohmic contact layer is removed by using the source 115a and drain electrode 115b as a mask (Fig. 11E).

Subsequently, the exposed portion of the semiconductor

layer is plasma-treated using N_2, O_2 or a gas containing N or F to form a surface treatment layer 136. Then, an protection layer made of an organic material such as BCB and PFCB is formed on the overall substrate 111 (Fig. 11F). A contact hole 131 is formed to expose the drain electrode 115b through the protection layer 126 over the drain electrode 115b. Next, ITO is deposited on the substrate including the protection layer 126 and patterned to form a pixel electrode 104, which makes an electrical contact with the drain electrode 115b and overlaps the data bus line 115 (Fig. 11H).

This embodiment is explained using IOP (ITO On Passivation) structure forming the pixel electrode 104 on the protection layer 126. However, this invention can be applied to TFTs having other structures, regardless of the sequence of the pixel forming steps. For example, the pixel electrode 104 may be formed before or after forming the source electrode 115a and the drain electrode 115b (Figs. 12A and 12B).

Further, as shown in Figs. 13 - 15, this invention can be applied to the staggered, coplanar and self-aligned structure of a TFT as well as the reversed stagger structure of a TFT shown in Fig. 11.

Thus, according to the present invention, the pixel electrode 104 can be formed to overlap part of TFT as well as the gate 117 and data bus line 115 as shown in Fig. 10,

thereby improving the aperture ratio.

Additionally, the pixel electrode 104 overlapping the gate bus line 117 can play a role as a storage capacitance electrode.

Example 2

Another example for the method of manufacturing the first substrate of an AMLCD is explained with reference to Fig. 16 showing a cross-sectional view taken along the line V-V in Fig. 10.

A metal layer, using Al, Al-Ta, Al-Mo, Ta or Ti (being able to be anodized) or Cr; is deposited on a transparent glass substrate 111 and patterned to form a gate bus line and gate electrode 117a branched off therefrom (FIG. 16A). When the metal layer is able to be anodized, an anodized layer 135 is formed on the gate bus line and the gate electrode 117a in order to improve the insulating property and to prevent hill-lock (Fig. 16B).

Then, the overall surface is deposited with an organic material such as BCB and PFCB to form a gate insulation layer, and plasma treated using N_2, O_2 or a gas containing N or F forming surface treatment layer 136a (Fig. 16C).

Then a-Si and n$^+$ a-Si are sequentially deposited on the organic insulating layer 123 and patterned together to form a semiconductor layer 122 and ohmic contact layer 125 (FIG. 16D). Next, a metal such as Al alloy is deposited on the ohmic contact layer 125 and patterned to form a data bus lines 115, a source electrode 115a branched off from the data line, and drain electrode 115b as an output terminal. The exposed portion of the ohmic contact layer is removed by using the source 115a and drain electrode 115b as a mask

(Fig. 16E).

Subsequently, the exposed portion of the semiconductor layer 122 is plasma-treated using N_2, O_2 or a gas containing N or F to form a surface treatment layer 136b. Then, an protection layer made of an organic material such as BCB and PFCB is formed on the overall substrate 111 (Fig. 16F).

A contact hole 131 is made to expose the drain electrode 115b through the protection layer 126 over the drain electrode 115b (Fig. 16G). Next, ITO is deposited on the substrate including the protection layer and patterned to form a pixel electrode 104, which makes an electrical contact with the drain electrode 115b and overlaps the data bus line 115 (Fig. 16H).

The plasma treatment of the organic gate insulating layer 123 and the semiconductor layer 122 using N_2, O_2 or a gas containing N or F modifies the surface bond structure of the organic layers so as to stabilize TFT ON characteristic without charge trap at the interface between the semiconductor layer 122 and the organic gate insulating layer 123 and to prevent detachment or patterning defects for the inorganic layers such as a metal, ITO and a-Si layers on the organic layer.

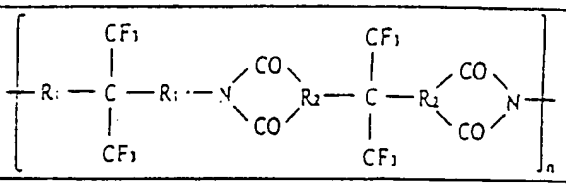
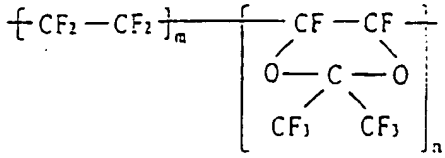
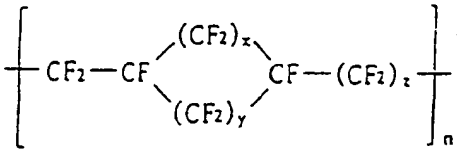
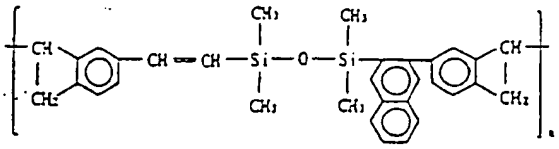
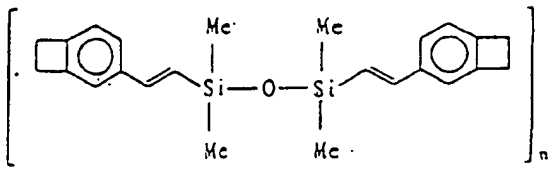
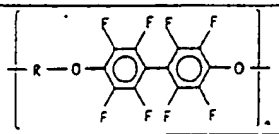
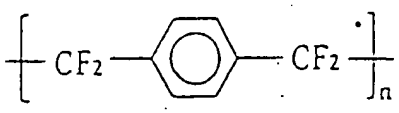
This embodiment is also explained using IOP (ITO On Passivation) structure forming the pixel electrode on the protection layer as in example 1. However, this invention can be applied to other structure of TFTs, regardless of the

sequence of the pixel forming step. For example, the pixel electrode 104 may be formed before or after forming the source 115a and drain 115b electrodes (Figs. 17A and 17B).

Thus, using the organic material such as BCB and PFCB for the gate insulating layer 123 and the protection layer 126, the plasma treatment of the organic insulating layer 123 and the semiconductor layer 122 allows an improved aperture ratio of the AMLCD with a stabilized TFT.

Similarly, a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether or fluorinated para-xylene, each having dielectric constant less than 3, may be used as the gate insulating layer 123 or the protection (passivation) layer 126, as shown in the Table 1.

Table 1. Dielectric Constant of organic materials

Organic material	Dielectric constant	Structure
Fluorinated polyimide	2.7	
Teflon	2.1 - 1.9	
Cytop	2.1	
BCB	2.7	 OR 
Fluoro-poly-arylether	2.6	
Fluorinated para-xylene	2.4	

Claims:

1. A method of manufacturing a liquid crystal display having a thin film transistor including a gate electrode branched off from a gate line, a first insulation layer covering the gate electrode, a semiconductor layer, an ohmic contact layer, and a source and a drain electrode branched off from a data bus line, and a second insulation layer covering the semiconductor layer, the method comprising the steps of:

surface-treating a surface of the semiconductor layer; and

forming the second insulation layer on the surface-treated surface of the semiconductor layer using an organic material.

2. The method according to claim 1, wherein the surface treatment step is a plasma treatment.

3. The method according to claim 2, wherein the plasma treatment step uses at least one of N_2, O_2, N containing gas and F containing gas.

4. The method according to claim 1, 2 or 3, wherein the first insulation layer is formed under the semiconductor layer and comprises an organic material.

5. The method according to claim 4, further comprising the step of surface-treating a surface of the first insulation layer.

6. The method according to claim 5, wherein the

surface treatment step is a plasma treatment.

7. The method according to claim 6, wherein the plasma treatment step uses at least one of N_2, O_2, N containing gas and F containing gas.

8. The method according to any one of claims 1 to 7, further comprising the step of forming a pixel electrode on the first or the second insulation layer.

9. The method according to claim 8, wherein the pixel electrode selectively overlaps the data bus line.

10. The method according to claim 8, wherein the pixel electrode selectively overlaps the data bus line and the gate bus line.

11. The method according to claim 8, 9 or 10, wherein the pixel electrode is formed before the formation of the source and drain electrodes.

12. The method according to claim 8, 9 or 10, wherein the pixel electrode is formed after the formation of the source and drain electrodes.

13. The method according to any one of claims 1 - 12, wherein the organic material includes Si-O bond structure.

14. The method according to any one of claims 1 - 13, wherein the organic material having a dielectric constant less than 3.0.

15. The method according to any one of claims 1 - 14, the organic material includes one of BCB, PFCB,

fluorinated polyimide, teflon, cytop, fluoropolyarylether and fluorinated para-xylene.

16. A liquid crystal display device comprising:

a thin film transistor including;

a gate electrode branched off from a gate line;

first insulation layer covering the gate electrode, a semiconductor layer;

an ohmic contact layer;

a source and a drain electrode branched off from a data bus line; and

a second insulation layer covering the semiconductor layer;

wherein a surface of the semiconductor layer is surface treated.

17. The device according to claim 16, wherein the surface treatment of the semiconductor layer is plasma treatment.

18. The device according to claim 17, wherein the plasma treatment uses at least one of N_2, O_2, N containing gas and F containing gas.

19. The device according to claim 16, 17 or 18, wherein the first insulation layer is formed under the semiconductor layer and uses an organic material.

20. The device according to claim 19, wherein a surface of the first insulation layer is surface treated.

21. The device according to claim 20, wherein the surface of the first insulation layer is plasma treated.

22. The method according to claim 21, wherein the plasma treatment uses at least one of N_2, O_2, N containing gas and F containing gas.

23. The device according to any one of claims 16 to 22, further comprising a pixel electrode on the first or the second insulation layer.

24. The device according to claim 23, wherein the pixel electrode selectively overlaps the data bus line.

25. The device according to claim 23, wherein the pixel electrode selectively overlaps the data bus line and the gate bus line.

26. The device according to claim 23, 24 or 25, wherein the pixel electrode is formed before the formation of the source and drain electrodes.

27. The device according to claim 23, 24 or 25, wherein the pixel electrode is formed after the formation of the source and drain electrodes.

28. The device according to any one of claims 16 - 27, wherein the organic material includes Si-O bond structure.

29. The device according to any one of claims 16 - 28, wherein the organic material has a dielectric constant less than 3.0.

30. The device according to any one of claims 16 -

29, the organic material includes one of BCB, PFCB, fluorinated polyimide, teflon, cytop, fluoropolyarylether and fluorinated para-xylene.

31. A method of manufacturing a semiconductor switching element, wherein a surface of the semiconductor layer and/or a surface of an organic insulating layer is/ are plasma treated such that said surface of the semiconductor layer/organic insulating layer has a stable bond structure.

32. A method according to claim 31, wherein the plasma treatment uses at least one of N_2, O_2, N containing gas and F containing gas.

33. A semiconductor switching element, wherein a surface of the semiconductor layer and/or a surface of an organic insulating layer is plasma treated such that said surface of the semiconductor layer/organic insulating layer has a stable bond structure.

34. A semiconductor switching element according to claim 33, wherein the plasma treatment uses at least one of N_2, O_2, N containing gas and F containing gas.

35. A method, semiconductor switching element or liquid crystal display device substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 6 to 17B of the accompanying drawings.

The Patent Office

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Application No: GB 9714111.3 **Examiner:** SJ Morgan
Claims searched: 1-35 **Date of search:** 6 October 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KCAA,KJACX,KJAX)

Int Cl (Ed.6): H01L

Other: Online:WPI,JAPIO,CLAIMS,INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,Y	EP 0 486 047 A2	(SEIKO) See line 1, column 5 - line 42, column 10.	X:16-18 & 31-34 Y:1-3
X,Y	US 5 281 546	(GENERAL ELECTRIC) See whole document.	X:16, 17, 31, & 33 Y:1-3
X	US 5 177 588	(MITSUBISHI) See line 8, column 5 - line 65, column 8.	31 & 33
X,Y	US 5 045 905	(NIPPON PRECISION CIRCUITS) See line 37, column 2 - line 61, column 3.	X:16-18 & 31-34 Y:1-3
X,Y	Patent Abstracts of Japan, Section P, Section No. 1476, Vol. 17, No. 45, Pg. 3, 28/1/93 & JP 4-257826A (SHARP). (See abstract).		X:31 & 33 Y:1-3

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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